

# INN100FQ016A

100V Enhancement-mode GaN Power Transistor

## INN100FQ016A

### 1. General description

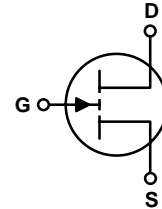
GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 4.0 mm x 6.0 mm package size.

### 2. Features

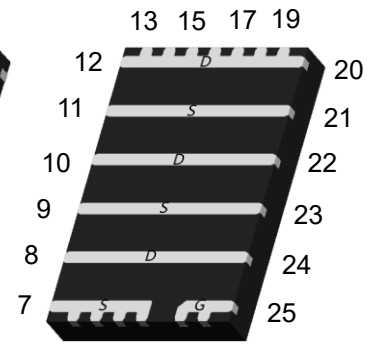
- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

### 3. Applications

- High frequency DC-DC converter
- Point of Load
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver



Top View



Bottom View

### 4. Key performance parameters

Table 1 Key performance parameters at  $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ $V_{GS} = 5\text{ V}$	1.8	m $\Omega$
$Q_{G,typ}$ @ $V_{DS} = 50\text{ V}$	22	nC
$I_{DS,Pulse}$	320	A
$Q_{OSS}$ @ $V_{DS} = 50\text{ V}$	125	nC

### 5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Source	Source
8,10,12-20,22,24	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100FQ016A	FCQFN 4X6	J23

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## 6. Maximum ratings

at  $T_J = 25\text{ °C}$  unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

**Table 4** Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage (up to 300,000 5ms pulse at 150 °C)	120	V
$I_D$	Continuous current	100	A
	Pulsed (25 °C, $T_{Pulse} = 100\ \mu s$ )	320	A
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	°C

## 7. Thermal characteristics

**Table 5 Thermal characteristics**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>TYP</b>	<b>UNIT</b>	<b>Note/Test Condition</b>
$R_{\theta JC}$	Thermal Resistance, Junction to Case	13.96	°C/W	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.92	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>1</sup>	57.56	°C/W	
$T_{sold}$	Maximum reflow soldering temperature	260	°C	MSL3

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

## 8. Electric characteristics

at  $T_J = 25\text{ }^\circ\text{C}$ , unless specified otherwise

**Table 6** Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$BV_{DSS}$	Drain-to-Source Voltage	100	-	-	V	$V_{GS} = 0\text{ V}$ , $I_D = 900\text{ }\mu\text{A}$
$I_{DSS}$	Drain Source Leakage	-	9.5	93	$\mu\text{A}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 80\text{ V}$
$I_{GSS}$	Gate-to-Source Forward Leakage	-	2.8	55	$\mu\text{A}$	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage	-	0.3	1.2	$\mu\text{A}$	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{DS} = V_{GS}$ , $I_D = 21\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance	-	1.4	1.8	$\text{m}\Omega$	$V_{GS} = 5\text{ V}$ , $I_D = 40\text{ A}$
$V_{SD}$	Source-Drain Forward Voltage	-	1.5	-	V	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$

**Table 7 Dynamic characteristics**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C <sub>ISS</sub>	Input Capacitance	-	2500	-	pF	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V
C <sub>OSS</sub>	Output Capacitance	-	1100	-		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V
C <sub>RSS</sub>	Reverse Transfer Capacitance	-	19	-		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V
C <sub>OSS(ER)</sub>	Energy Related C <sub>OSS</sub>	-	1700	-		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 V to 50 V
C <sub>OSS(TR)</sub>	Time Related C <sub>OSS</sub>	-	2500	-		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 V to 50 V
R <sub>G</sub>	Gate resistance	-	1.8	-	Ω	f = 5 MHz, open drain
Q <sub>G</sub>	Total Gate Charge	-	22	-	nC	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 50 V, I <sub>D</sub> =40 A
Q <sub>GS</sub>	Gate to Source Charge	-	4.5	-		V <sub>DS</sub> = 50 V, I <sub>D</sub> =40 A
Q <sub>GD</sub>	Gate to Drain Charge	-	4.5	-		V <sub>DS</sub> = 50 V, I <sub>D</sub> =40 A
Q <sub>G(TH)</sub>	Gate Charge at Threshold	-	2.5	-		V <sub>DS</sub> = 50 V, I <sub>D</sub> =40 A
Q <sub>OSS</sub>	Output Charge	-	125	-		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V

### 9. Electric characteristics diagrams

at  $T_J = 25\text{ }^\circ\text{C}$ , unless specified otherwise

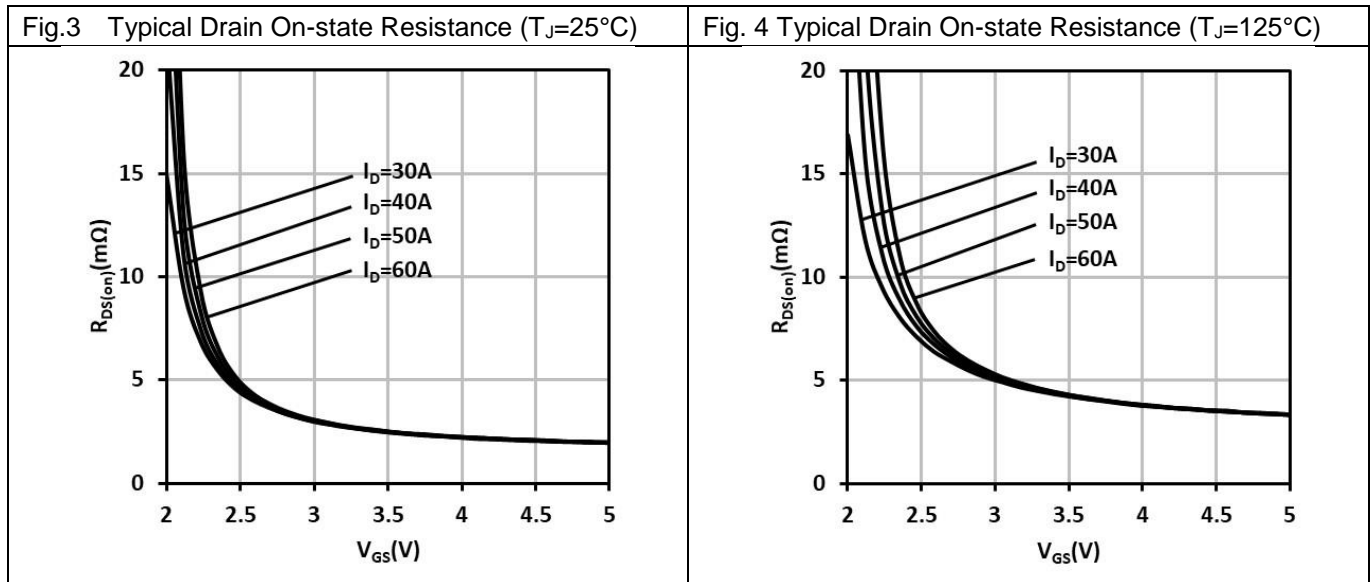
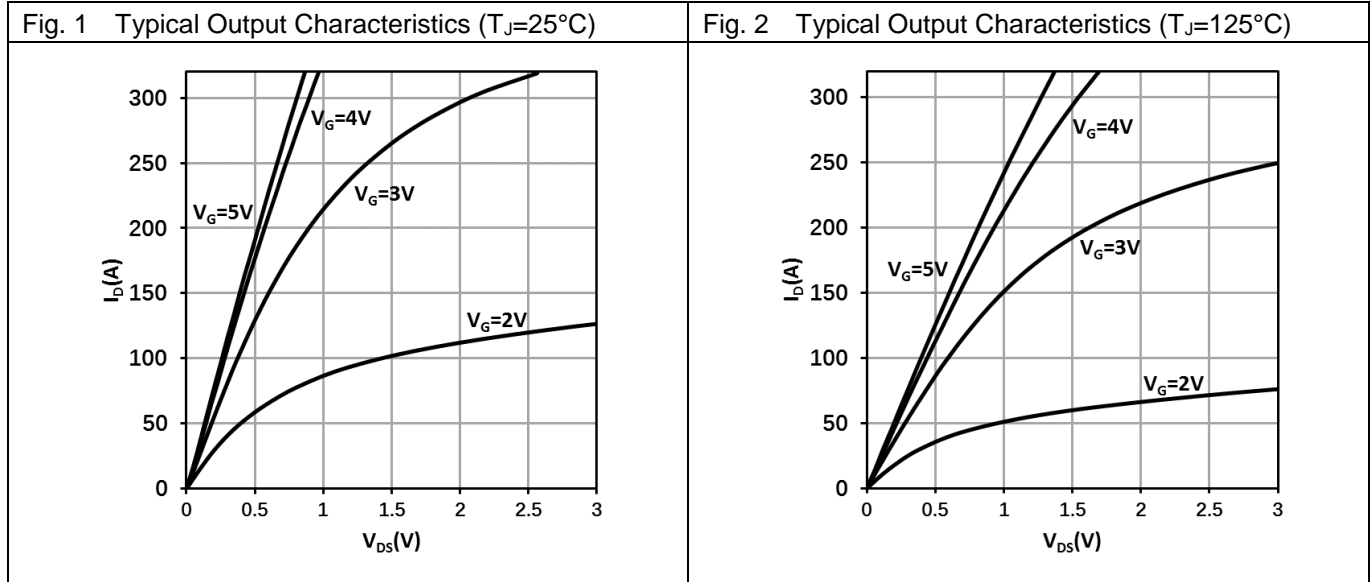


Fig. 5 Normalized On-State Resistance vs. Temp.

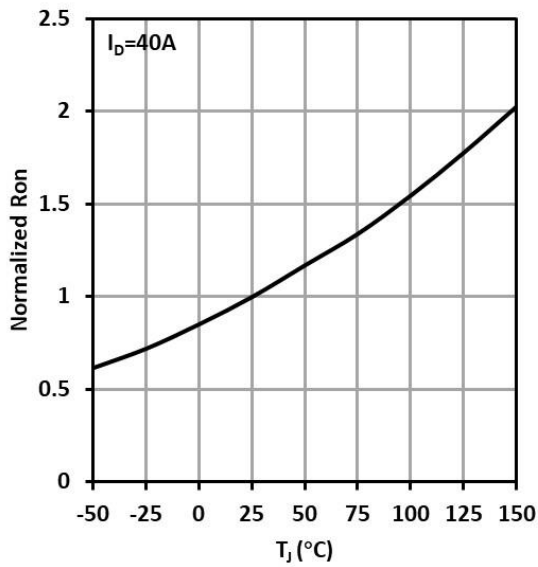


Fig. 6 Typical Transfer Characteristics

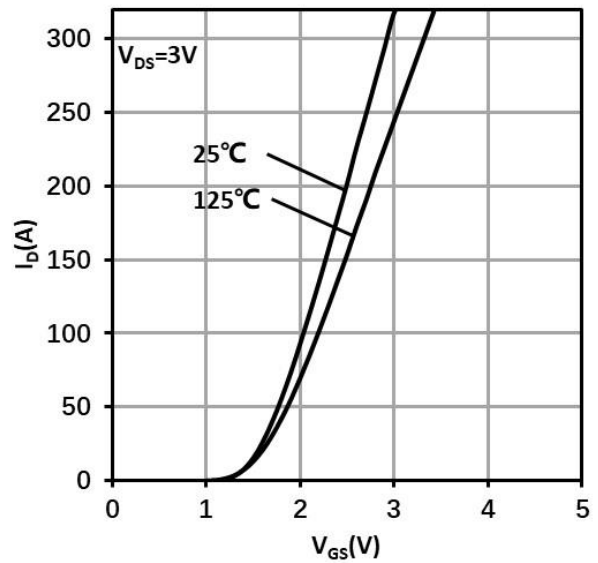


Fig. 7 Typ. Reverse Drain-Source Characteristics ( $V_{GS} \leq 0, T_J = 25^\circ\text{C}$ )

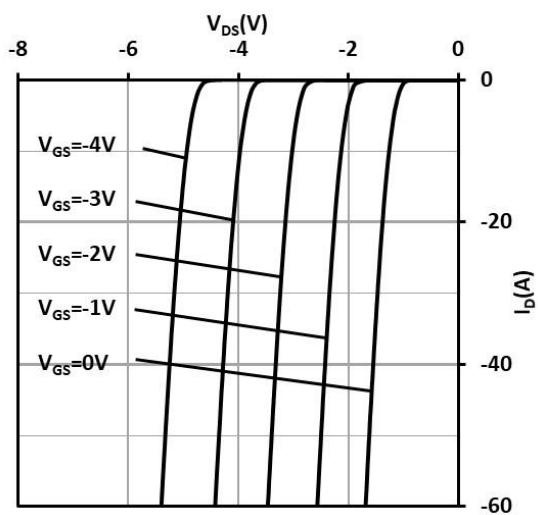


Fig. 8 Typ. Reverse Drain-Source Characteristics ( $V_{GS} \geq 0, T_J = 25^\circ\text{C}$ )

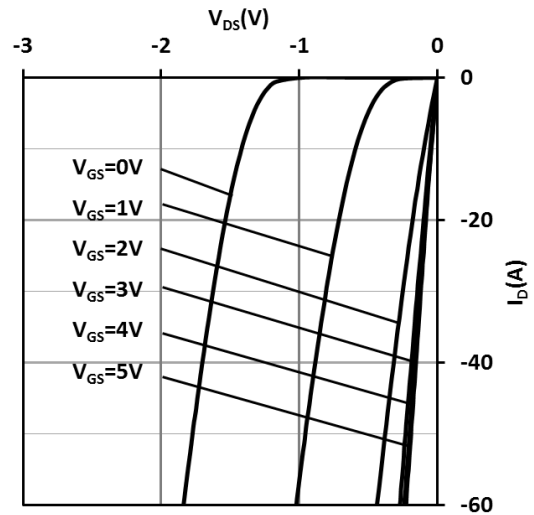




Fig. 9 Typ. Reverse Drain-Source Characteristics ( $V_{GS} \leq 0, T_J = 125^\circ\text{C}$ )

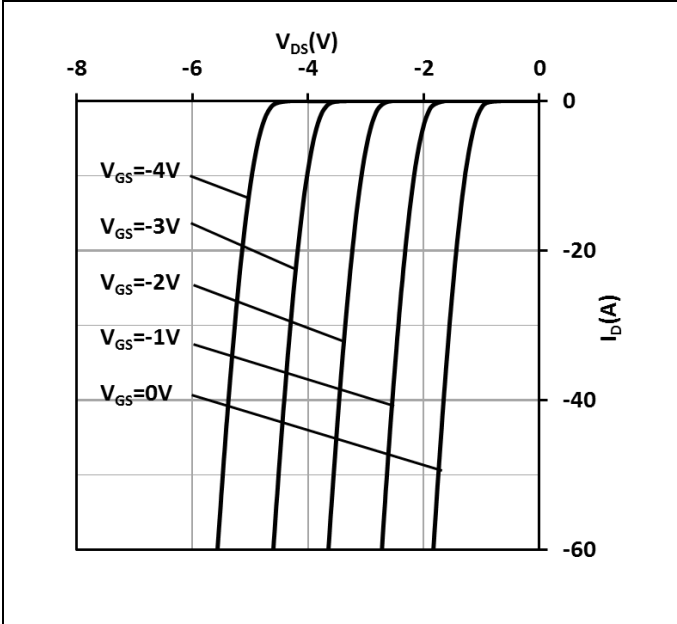


Fig. 10 Typ. Reverse Drain-Source Characteristics ( $V_{GS} \geq 0, T_J = 125^\circ\text{C}$ )

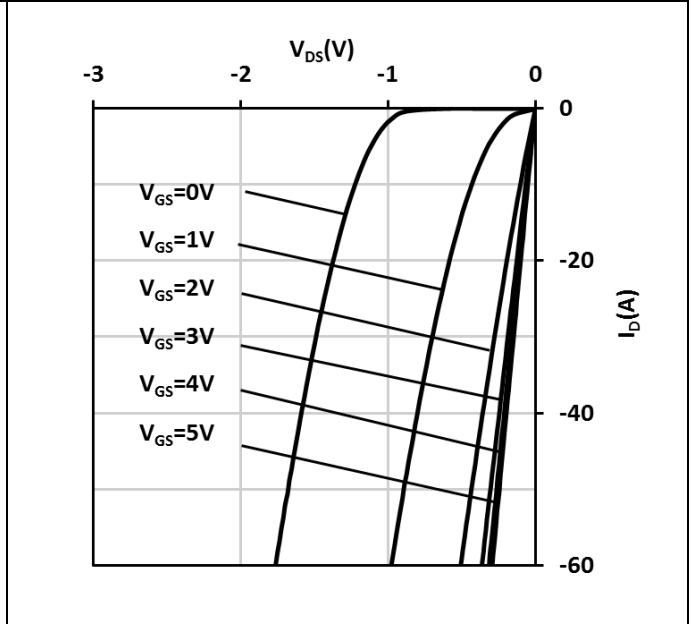


Fig. 11 Typ. Capacitances Characteristics

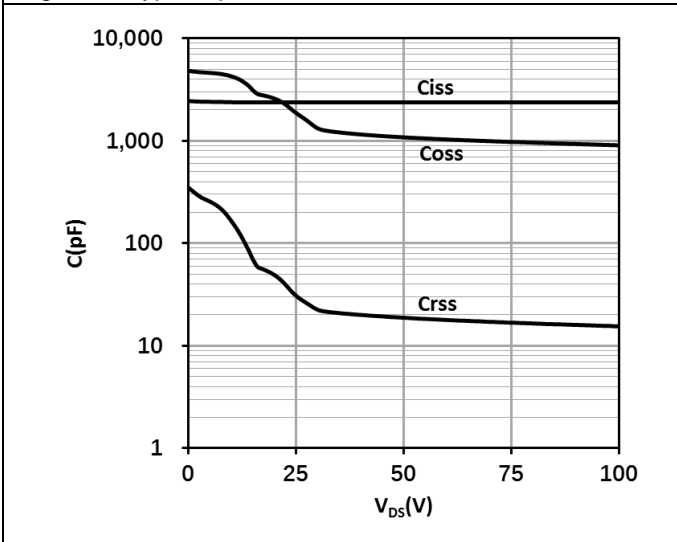


Fig. 12 Typ. Gate Charge

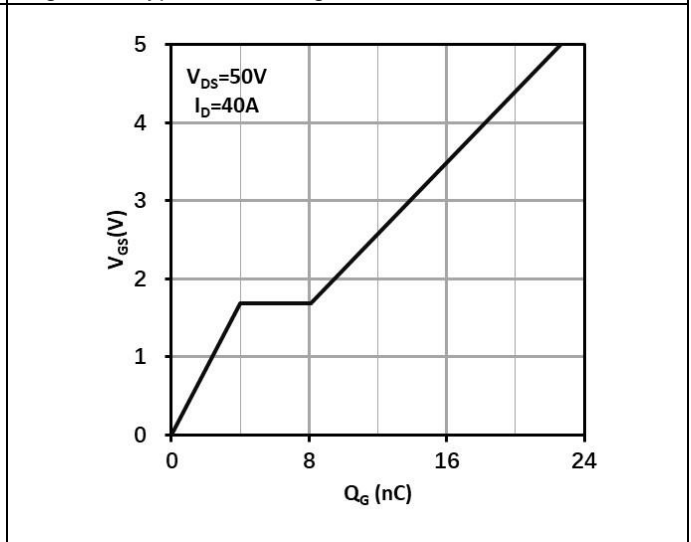


Fig. 13 Normalized Threshold Voltage vs. Temp.

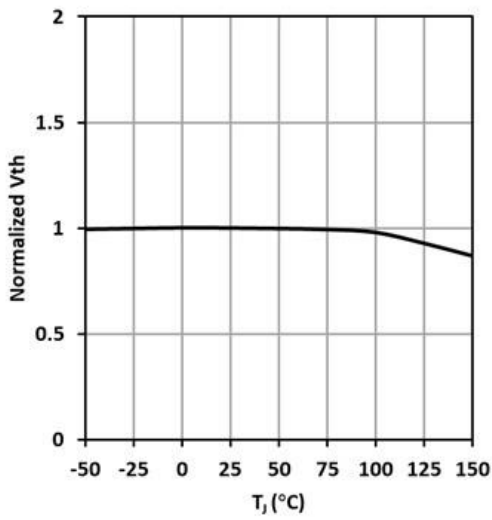


Fig. 14 Output Charge

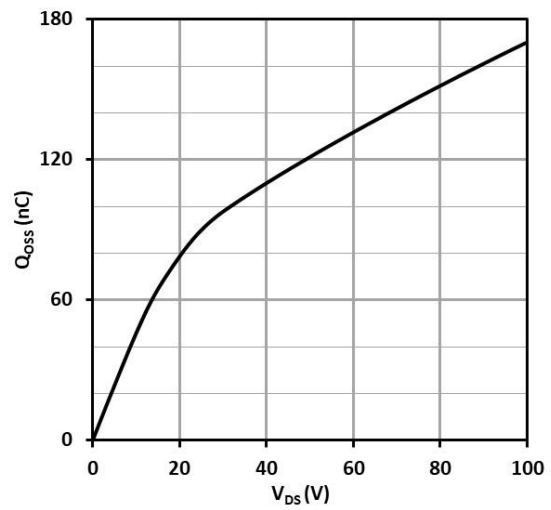


Fig. 15 Output Capacitance Stored Energy

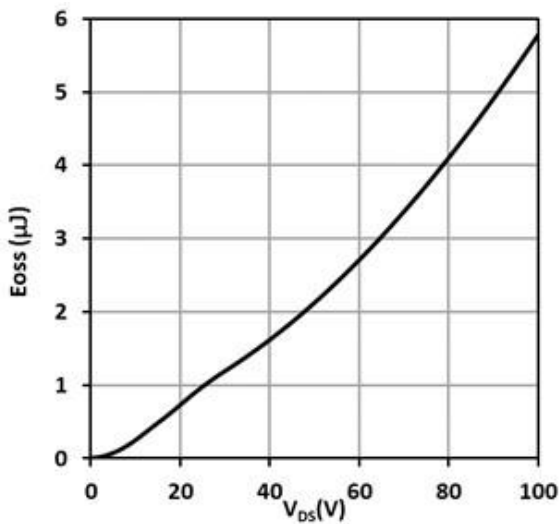


Fig. 16 Power Dissipation

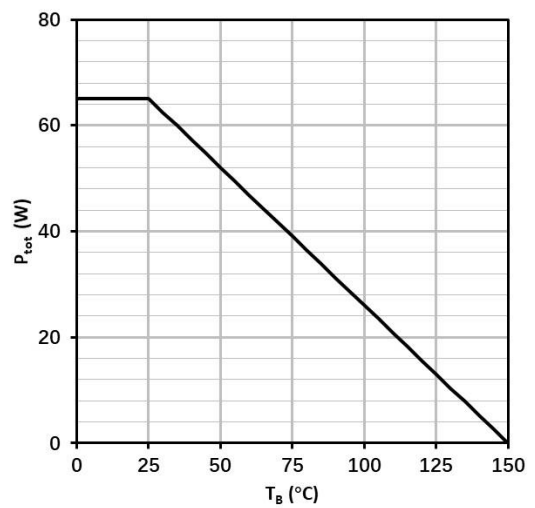


Fig. 17 Safe Operating Area

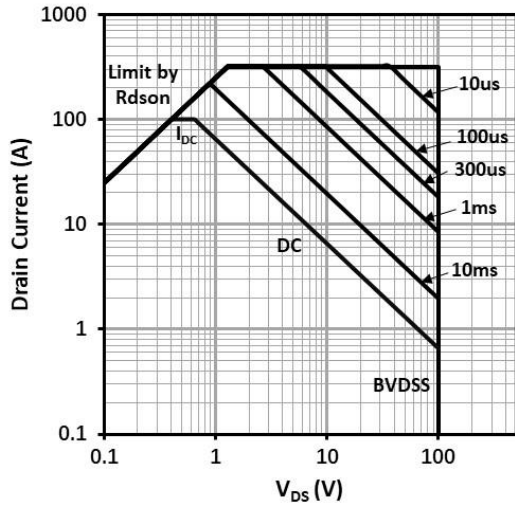
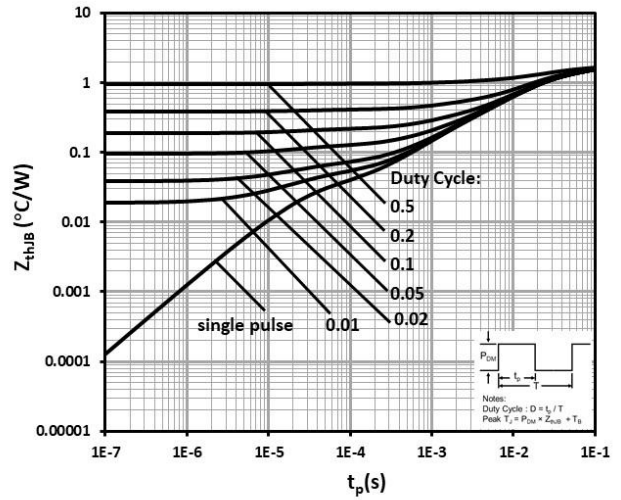
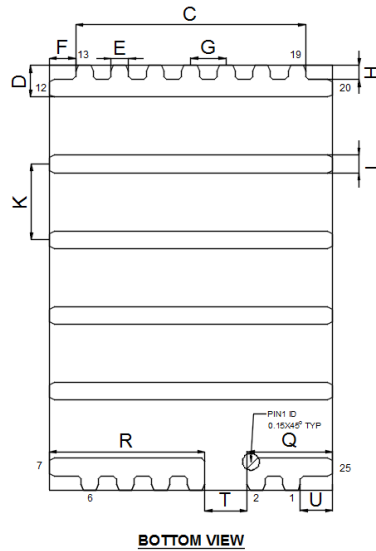
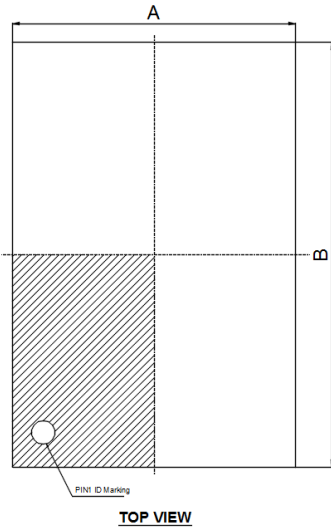


Fig. 18 Max. Transient Thermal Impedance

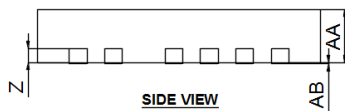


### 10. Package outlines

#### Package Reference

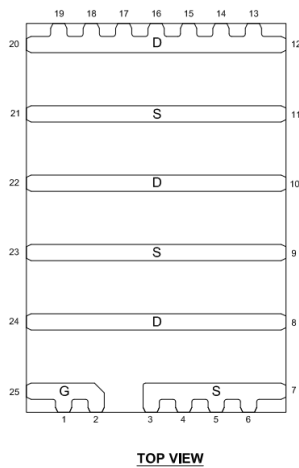


SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	5.9	6.0	6.1	
C	3.15	3.25	3.35	
D	0.35	0.45	0.55	3X
E	0.20	0.25	0.30	13X
F	0.375 REF			2X
G	0.5 BASIC			10X
H	0.2 REF			3X
K	1.07 BASIC			6X
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
T	0.55	0.60	0.65	
U	0.45 REF			2X
Z	0.203 REF			7X
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	

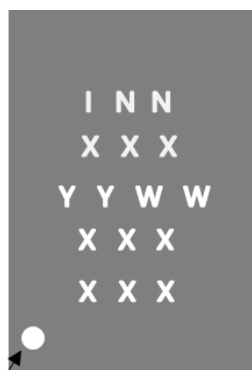


**NOTE:**  
 1) ALL DIMENSION ARE IN MILLIMETERS.  
 2) BOTTOM VIEW IS FT TESTER SIDE VIEW.  
 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.  
 4) COMPLIES WITH JEDEC MO-220.  
 5) DRAWING IS NOT TO SCALE.

#### Pin information:



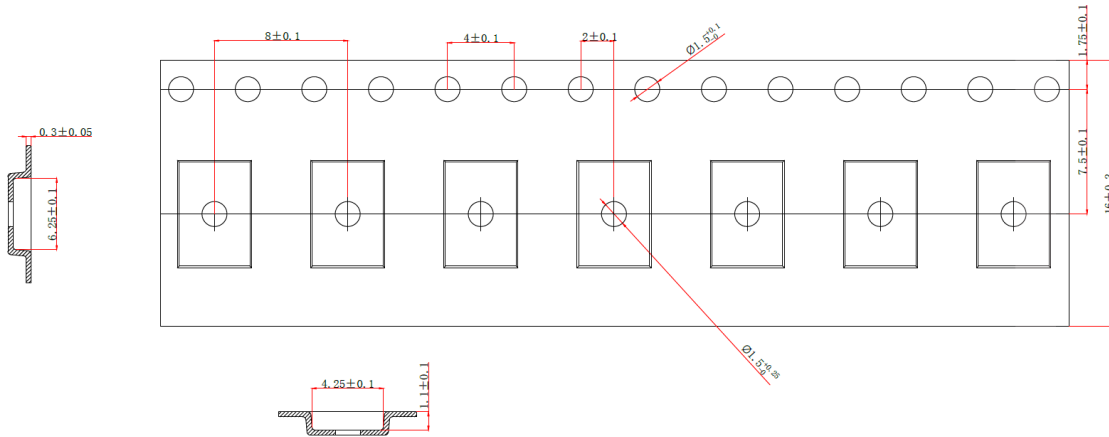
#### Marking Reference:



Die Orientation Dot  
& Gate Position

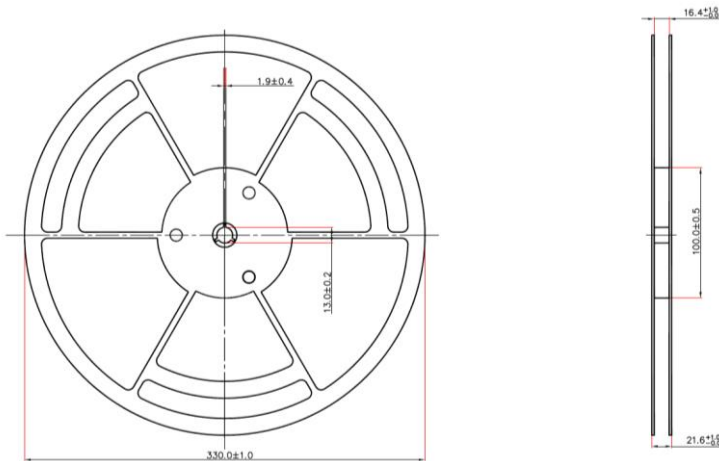
Row <sup>⌄</sup>	Description <sup>⌄</sup>	Example <sup>⌄</sup>
Row 1 <sup>⌄</sup>	Company name <sup>⌄</sup>	INN <sup>⌄</sup>
Row 2 <sup>⌄</sup>	Product code <sup>⌄</sup>	XXX <sup>⌄</sup>
Row 3 <sup>⌄</sup>	Date code <sup>⌄</sup>	YYWW <sup>⌄</sup>
Row 4 <sup>⌄</sup>	Lot No <sup>⌄</sup>	XXX <sup>⌄</sup>
Row 5 <sup>⌄</sup>	Lot No <sup>⌄</sup>	XXX <sup>⌄</sup>

### 11. Reel information



**NOTES:**

1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.

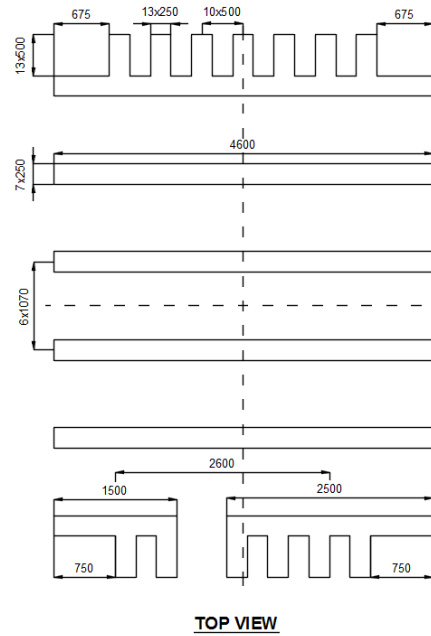


**NOTES:**

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

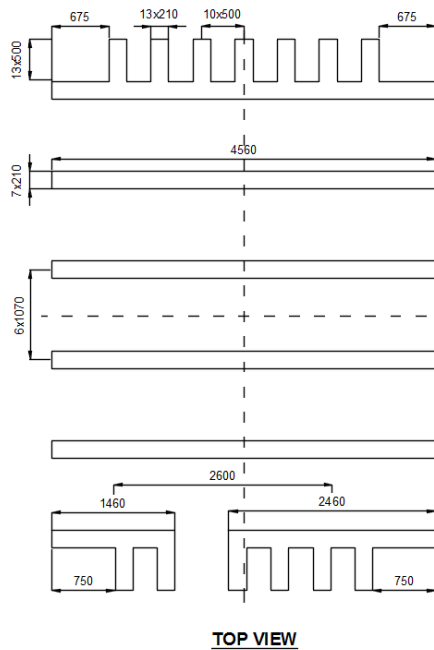
## 12. Land pattern

### Recommended land pattern



Unit:  $\mu\text{m}$

### Recommended Stencil drawing



Unit:  $\mu\text{m}$

### 13. Revision history

**Major changes since the last revision**

Revision	Date	Description of changes
1.0	2023-07-19	Version 1.0 release
1.1	2023-12-19	Update thermal resistance & SOA
1.2	2024-03-04	Add $V_{DS(tr)}$ in table 4

## Important Notice

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